



R20 Regulation

Subject code:3E5DA

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Supplementary Examinations, May 2025

DIGITAL DESIGN THROUGH VERILOG HDL

(ECE)

Maximum Marks: 70

Date: 27.06.2025

Duration: 3 hours

- Note: 1. This question paper contains two parts A and B.
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	Explain simulation and synthesis with differences.	2M	1	L1
2	Mention data types used in Verilog HDL.	2M	1	L1
3	Illustrate with an example Array of Instances of Primitives.	2M	2	L1
4	Write a Verilog code for half adder.	2M	2	L1
5	Define gate delays with example.	2M	3	L1
6	Write about Arithmetic operators in Verilog.	2M	3	L1
7	Illustrate about Test Benches.	2M	4	L1
8	Compare sequential and parallel blocks.	2M	4	L1
9	Define task with an example.	2M	5	L1
10	Write a syntax for \$monitor.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Illustrate the application of Verilog HDL by discussing the various modeling styles and providing examples for each.	10M	1	L2
OR				
12	Compare logic values and strengths in verilog HDL with one example.	10M	1	L2
13	Create a comprehensive plan for constructing full subtractor by using Gate level modeling.	10M	2	L2
OR				
14	Synthesize an in-depth analysis of the strengths associated with contention resolution in Verilog.	10M	2	L2
15	Critically assess and categorize different operands and operators in Verilog HDL.	10M	3	L2
OR				
16	Design and develop Verilog code for 2-Input NAND gate using CMOS switches.	10M	3	L2

17	Design 4 X 1 multiplexer using if else construct.	10M	4	L2
	OR			
18	Design and develop Verilog code for 2 to 4 decoder in Behavioral modeling.	10M	4	L2
19	Differentiate between tasks and Functions using one example	10M	5	L2
	OR			
20	Distinguish Combinational and sequential UDPs.	10M	5	L2